AMENDMENTS TO THE SPECIFICATION

Page 1:

Please substitute the following paragraph for the paragraph beginning at line 6:

C1

The present invention relates to a semiconductor device and a method of manufacturing the same and particularly to a semiconductor device having the function to control the threshold voltage of a transistor formed in ~~the~~ a well through the ON/OFF control of a switch element provided between the power supply wiring and the well and a technique which may be effectively adapted to the design of the same semiconductor device.

Please substitute the following paragraph for the paragraph beginning at line 16:

C2

With the requirements for scale-down of a semiconductor element, low power consumption of a semiconductor device and improvement in the operation ~~rate~~ speed of a semiconductor device, the threshold voltage of a transistor in a semiconductor device has been lowered. However, because of a low threshold voltage, there arises a problem that it is difficult to determine ~~that~~ if a true fault is generat d ~~or not~~ on the occasion of inspecting

C2 whether a leak current is generated ~~or not~~ between the source and drain of a transistor of the semiconductor device. Moreover, a problem generated when a semiconductor device is in the condition for waiting ~~the~~ operation is that the power consumption increases with a leak current of transistor. In order to overcome such problem, a technology has been proposed in which the threshold voltage of transistor is temporarily raised to reduce a leak current by applying ~~the~~ a predetermined voltage to the semiconductor substrate where transistors are arranged (in more practical terms, semiconductor region called a well). Thereby, for example, during the testing period, when the transistor is turned ON even if the threshold value is raised, such transistor can be determined as a defective one. Moreover, when the semiconductor device is in the condition for waiting ~~the~~ operation, a leak current can be reduced and power consumption of the semiconductor device can also be lowered through increase of the threshold voltage of transistor. The technique for varying this threshold voltage is described, for example, in the NIKKEI MICRODEVICE (Aug., 1996), pp. 50–66 (issued on Aug. 1, 1996), NIKKEI BP, Inc. Namely, a circuit structure and an element layout structure are disclosed for the technique to

C2 change the threshold voltage through the feedback control of substrate voltage and to realize low power consumption and high-speed operation.

Page 4:

C3 Please substitute the following paragraph for the paragraph beginning at line 21:

~~The typical inventions~~ Exemplary aspects of the present invention disclosed in this specification ~~will~~ may be summarized as follows.

Page 13:

Please substitute the following paragraph for the paragraph beginning at line 24:

C4 Fig. 1 is an explanatory diagram illustrating the technique discussed ~~with~~ by the inventors of the present invention.

Page 14:

Please substitute the following paragraph for the paragraph beginning at line 10:

C5

Fig. 5 is an explanatory diagram schematically illustrating a circuit of the technique discussed ~~with~~ by the inventors of the present invention.

Page 15:

Please substitute the following paragraph for the paragraph beginning at line 15:

C6

Fig. 16 is a plan view of ~~the essential~~ a principal portion of a semiconductor substrate where the basic cells among the element layout of Fig. 15 are extracted.

Please substitute the following paragraph for the paragraph beginning at line 22:

C7

Fig. 19 is a plan view of ~~the essential~~ a principal portion of a semiconductor substrate illustrating an example of the case where the wirings are laid on the semiconductor substrate of Fig. 15.

Please substitute the following paragraph for the paragraph beginning at line 26:

C8 Fig. 20 is a plan view of ~~the essential~~ a principal portion of a semiconductor substrate in the case where only the first layer and second layer wirings are arranged on the semiconductor substrate in the semiconductor device of Fig. 19.

Page 16:

Please substitute the following paragraph for the paragraph beginning at line 4:

C9 Fig. 21 is a plan view of ~~the essential~~ a principal portion of a semiconductor substrate in the case where only the first layer and second layer wirings are arranged on the semiconductor substrate in the semiconductor device of Fig. 19.

Page 17:

Please substitute the following paragraph for the paragraph beginning at line 5:

C10 Fig. 31 is a plan view of ~~the essential~~ a principal portion illustrating allocation of the wiring system and

circuit system in the periphery of external circumference of the semiconductor device of Fig. 6.

Please substitute the following paragraph for the paragraph beginning at line 9:

Fig. 32 is an enlarged plan view of ~~the essential~~ a principal portion of Fig. 31.

Please substitute the following paragraph for the paragraph beginning at line 14:

Fig. 34 is a plan view of ~~the essential~~ a principal portion of the semiconductor substrate illustrating an element layout example of the input/output circuit cells of Fig. 33.

Page 27:

Please substitute the following paragraph for the paragraph beginning at line 14:

A switch element ~~3SW2~~ 3SW1 is provided between the power supply wiring 2VDD and the wiring 2VPP (n-well) and a switch element 3SW2 is provided between the power supply wiring 2VSS and the wiring 2VNN (p-well). These switch elements ~~2SW1~~ 3SW1, 3SW2 electrically connect or disconn ct

the power supply wirings 2VDD, 2VSS and wirings 2VPP, 2VNN (well). Namely, when the switch elements 3SW1, 3SW2 are in the ON condition, the voltages of the n-well and p-well are set to the power supply voltages (n-well is power supply voltage VDD, p-well is power supply voltage VSS) and the bias voltage is not applied to each well. Meanwhile, under the condition that the switch elements 3SW1, 3SW2 are in the OFF condition, the bias is generated in each well by externally applying the voltage different from the power supply voltage to the wirings 2VPP, 2VNN (n-well and p-well).

C13

Page 29:

Please substitute the following paragraph for the paragraph beginning at line 26:

C14

Moreover, the third distinctive characteristic of the technical concept of the present invention is that the semiconductor region of the unused transistor region and the power supply are electrically connected to form a diode capacitance C2b as the capacitance element. Namely, as illustrated in Fig. 4, the semiconductor region (drain) of pMISQp of unused basic cell 1 (UU) and the power supply wiring 2VDD are electrically connected and moreover the

C14 semiconductor region (source) of nMISQn of unused basic cell 1 and the power supply wiring 2VSS are electrically connected. Thereby, even in the region of unused basic cell 1 (UU), a diode capacitance C2b corresponding to the diode capacitance C2 is formed between the power supply wiring 2VDD and wiring 2VPP(n-well) and between the power supply wiring 2VSS and the wiring 2VNN (p-well). Namely, the capacitance element (diode capacitance element) C2 is formed using the unused basic cell 1 (UU) not forming a logic circuit. Thereby, since the diode capacitance C2 can be increased without deterioration of the area efficiency in the semiconductor device, noise of well can be reduced. As illustrated in Fig. 5, since the basic cell not forming the logic circuit is not electrically connected to the power supply wirings 52VDD, 52VSS, the diode capacitance C2b is not formed.

Page 31:

Please substitute the following paragraph for the paragraph beginning at line 11:

C15 The semiconductor chip 4 is formed in the manner, for example, that a small piece of a square flat silicon single crystal is used as the element forming member and a

C 15 plurality of basic cells ~~2~~ 1 are regularly arranged along the X direction and Y direction at the center of the main surface (internal circuit region). Namely, the gate array in this embodiment is a so-called SOG (Sea Of Gate) type or channel-less type gate array. However, the present invention is not limited only to application into the SOG type gate array and allows various changes and modifications. For example, the present invention can also be adapted to the ordinary gate array wherein the basic cell train allocating a plurality of basic cells ~~2~~ 1 along the X direction is provided in the plural trains via the wiring channel and to the composite type gate array wherein ROM (Read Only Memory) and RAM (Random Access Memory) or the like are also arranged in addition to the basic cells 1 in the internal circuit region.

Page 34:

Please substitute the following paragraph for the paragraph beginning at line 7:

C 16 The semiconductor regions (drains) of pMISQp for a plurality of switch elements 3SW1 dispersed within the same n-well NWL are electrically connected with each other via the power supply wiring 2VDDA ~~and~~ which is electrically

connected to the power supply wiring 2VDDB arranged surrounding the external circumference of the internal circuit region A. Moreover, the semiconductor regions (sources) of the pMISQp of a plurality of switch elements 3SW1 are electrically connected to the n-well NWL via the wiring 2VPPA. As explained above, a switch element 3SW1 is provided between the power supply wiring 2VDDB and n-well NWL. The wiring 2VPPB arranged to surround the external circumference of the internal circuit region A is electrically connected to the n-well NWL so that the predetermined voltage can be applied to the n-well NWL from the external circuit.

Page 36:

Please substitute the following paragraph for the paragraph beginning at line 3:

Moreover, in this embodiment, the I/O cells are divided for the internal region side and external region side with a broken line B of Fig. 7 defined as the ~~boarder~~ border line and the switch elements 3SW3, 3SW4 are formed of the elements in the internal region side. These switch elements 3SW3, 3SW4 have the same function as that of the switch elements 3SW1, 3SW2 in the internal circuit region

A. It is because the element (MISFET) in the internal region side of the I/O cell 5 mainly forms the input circuit as will be explained later and therefore the threshold voltage must be lowered relatively in the same size as the element (MISFET) of the internal circuit region A in order to ~~improvement in~~ improve the operation rate and therefore it is required to change the threshold voltage at the time, for example, of electrical testing and waiting period of the semiconductor device. Since these switch elements 3SW3, 3SW4 are provided, it is now possible, during the normal operation, to turn ON the switch elements 3SW3, 3SW4 to lower the threshold value of the MISFET in the internal region of I/O cell 5 as specified and also possible, during the inspection period, to turn OFF the switch elements 3SW3, 3SW4 to relatively raise the threshold value of the MISFET in the internal region of the I/O cell 5.

Page 37:

Please substitute the following paragraph for the paragraph beginning at line 1:

In this embodiment, these switch elements 3SW3, 3SW4 ar unused pMISQpA and nMISQnA in the internal region of

C18

the I/O cell 5. However, the switch elements 3SW3, 3SW4 may also be formed of the unused elements in the I/O cell 5. In Fig. 7, the switch elements 3SW3, 3SW4 are arranged at the area near the angled corners of the semiconductor chip 4 and it is also possible to provide a plurality of switch elements 3SW3, 3SW4 to each side of the semiconductor chip 4. However, in this case, it is not enough to arrange only the switch elements 3SW3, 3SW4 but it is required to give any adverse effect on the allocation of the input/output circuits and to consider a certain means to reduce the well noise. The layout in the I/O cell 5 and effect of the switch element will be explained later in detail.

Page 38:

Please substitute the following paragraph for the paragraph beginning at line 23:

C19

Application examples of such switch element will be explained with reference to Fig. 9 to Fig. 11. In Fig. 9 and Fig. 11, the switch elements ~~2SW1, 2SW2~~ 3SW1, 3SW2 are indicated with the electrical code of the switch in order to make obvious the ON/OFF conditions of the switch elements 3SW1, 3SW2.

Page 39:

Please substitute the following paragraph for the paragraph beginning at line 2:

C20

Fig. 9 schematically illustrates the condition of the electric testing such as the measuring inspection of standby current in the semiconductor device of this embodiment. During the testing, the switch elements 3SW1, 3SW2 are turned OFF with the signal from the wirings 2VDBC, 2VSBC and the predetermined voltages VPP, VNN different from the power supply voltages VDD, VSS are applied to the wirings 2VPP, 2VNN (well) from a tester 6 (namely, from the external side of the semiconductor chip 4) under the condition that the power supply wiring ~~wVDD~~ 2VDD and wiring 2VPP (n-well) are electrically separated and the power supply wiring 2VSS and the wiring 2VNN (p-well) are electrically separated. Thereby, it is now possible to set the threshold voltage of pMISQp and nMISQn in the basic cell 1 to the predetermined value (relatively higher value for that in the operating condition) different from that in the operating condition. In this testing, the predetermined voltages VPP, VNN are applied across the n-well NWL or p-well PWL as illustrated in Fig. 10. However, in this testing, a logic circuit is not operated and noise

C28 level is not a problem and therefore the diffusing resistors R2n, R2p may have higher resistance values. Moreover, the power supply voltage VDD during the testing is, for example, about 3.5 V and the power supply voltage VSS is, for example, about -1.8V. Therefore, a leak current can be lowered by increasing the threshold value of the transistor during the testing and thereby it can be determined easily whether a transistor is defective or not.

Page 44:

Please substitute the following paragraph for the paragraph beginning at line 25:

C29 Fig. 15 is a flat layout diagram of ~~the essential~~ a principal portion of the CMIS gate array of this embodiment. Fig. 16 is a flat layout diagram where only the basic cell 1 is extracted from Fig. 15. Moreover, Fig. 17 is a cross-sectional view along the line XA-XA of Fig. 15 and Fig. 18 is a cross-sectional view along the line XB-XB of Fig. 15. The codes CHX and CHY in Fig. 15 and Fig. 16 are the wiring pitch line (namely, wiring channel (wiring route)) and these are not formed in the actual product. A cross mark is given to the intersecting points of the wiring pitch lines CHX, CHY and the contact hole is

C 20 arranged at the position of this cross to connect between the wiring and semiconductor substrate and between different wiring layers. One pitch of the wiring pitch line is, for example, about 0.5μm. As is illustrated in Fig. 16, the basic cell 1 is formed, in the Y direction (direction perpendicular to the X direction), of two nMIS forming regions QNA and ~~tow~~ two pMIS forming regions QPA, but the present invention is not limited thereto and it is also possible that the basic cell 1 is formed, in the Y direction, of one nMIS forming region QNA and one pMIS forming region QPA.

Page 47:

Please substitute the following paragraph for the paragraph beginning at line 11:

C 21 The pMIS forming region QPA is arranged on the n-well NWL and each region thereof is formed, for example, of two pMISQp, Qp. Each pMISQp includes, as explained above, a pair of semiconductor regions 8P to form the source and drain, a gate insulation film 9 and a gate electrode 10. Here, two gate electrodes 10 are arranged in flat with the overlapping manner in the two active regions for pMISQp, Qp and the semiconductor region 8P between the adjacent gate

C2 electrodes 10, 10 is formed as the common region for the two pMISQp, Qp. In the semiconductor region 8P, boron, for example, is included. Here, it is also possible to provide a so-called LDD (Lightly Doped Drain) structure which suppresses the hot carrier by forming the semiconductor region 8P with the low impurity concentration region arranged in the channel side of MISFET and the high impurity concentration region formed at the position isolated as much as the low impurity concentration region from the channel electrically connected to such low impurity concentration region. Moreover, it is also possible to form the structure to suppress the punch-through between the source and drain by providing the semiconductor region in the conductivity type different from that of the semiconductor region 8P at the position in the predetermined depth from the main surface of the semiconductor substrate at the region near the end part of channel side of the semiconductor region 8P.

Page 51:

Please substitute the following paragraph for the paragraph beginning at line 6:

C23

Next, a structure including the wirings of the semiconductor device will be explained with reference to Fig. 19 to Fig. 24. Fig. 19 illustrates an example where the first to third wiring layers are arranged on the layout of Fig. 15. Moreover, Fig. 20 illustrates an example where the first wiring layer and second wiring layer are arranged. Moreover, Fig. 21 illustrates allocation of only the first wiring layer. Moreover, Fig. 22 is a cross-sectional view along the line XA-XA of Fig. 21. Moreover, Fig. 23 is a circuit diagram of the switch element illustrated in Figs. ~~29~~ 19 to 23. Moreover, Fig. 24 is a cross-sectional view along the line XB-XB of Fig. 19.

Page 53:

Please substitute the following paragraph for the paragraph beginning at line 8:

C24

Moreover, the other semiconductor region 8P of pMISQp forming the switch element 3SW1 (at the center in the width direction of the active region L) and the n+ type semiconductor region 14N (nam ly, n-well NWL) adjacent to

C 24

such pMISQp are electrically connected via the wiring 2VPPA1 of the first layer (corresponding to the wiring 2VPPA) and the contact hole 15e arranged at the area near ~~the~~ both ends thereof. Thereby, the power supply wiring 2VDDA1 of the first layer and the n-well NWL are connected via two pMISQps for switch element ~~2SW1~~ 3SW1. Moreover, the gate electrodes 10, 10 of two pMISQp forming the switch element 3SW1 are electrically connected via the wiring 2VDBCA1 of the first layer and the contact hole 15f arranged at the area near both ends thereof.

Please substitute the following paragraph for the paragraph beginning at line 23:

C 25

In addition, the other semiconductor region 8N of nMISQn forming the switch element ~~2SW2~~ 3SW2 (at the center in the width direction of the active region L) and the p+ type semiconductor region 14P adjacent to such nMISQn (namely, the p-well PWL) are electrically connected via the wiring 2VNNA1 of the first layer (corresponding to the wiring 2VNNA) and the contact hole 15e arranged at the area near both ends thereof. Therefore, the power supply wiring 2VSSA1 of the first layer and p-well PWL are connected via two nMISQns for switch element 3SW2. Moreover, the gate

C25 electrodes 10, 10 of two nMISQns forming the switch element 3SW2 are electrically connected via the wiring 2VSBCA1 of the first layer and the contact hole 15f arranged at the area near both ends thereof. As illustrated in Fig. 23, the switch element 3SW1 includes two pMISQps, while the switch element 3SW2 includes two nMISQns.

Page 56:

Please substitute the following paragraph for the paragraph beginning at line 2:

C26 Moreover, the wirings 2VDBCA2, 2VSBCA2 of the second layer are used to transmit the control signal to turn ON and OFF the switch elements 3SW1, 3SW2 and are extended like a belt along the Y direction. The wiring 2VDBCA2 is electrically connected to the wiring 2VDBCA1 of the first layer via the contact hole 15k and thereby electrically connected to the gate electrodes 10, 10 of two pMISQps for switch element 3SW1~~are~~. On the other hand, the wiring 2VSBCA2 is electrically connected to the wiring 2VSBCA1 of the first layer via the contact hole 15m and thereby electrically connected to the gate electrodes 10, 10 of two nMISQns for switch element 3SW2.

Please substitute the following paragraph for the paragraph beginning at line 15:

Moreover, the wirings 2VDBCA3 and 2VSBCA3 are formed on the third wiring layer. Here, the wirings of the third wiring layer are arranged to extend along the X direction. These wirings 2VDBCA3, ~~2VDSBCA3~~ 2VSBCA3 are used to transmit the control signal to turn ON and OFF the switch elements ~~2SW1~~ 3SW1, 3SW2 and are extended like belts in parallel to the power supply wirings 2VDDA1, 2VSSA1 of the second layer along the X direction. The wiring 2VDBCA3 is electrically connected to the wiring 2VDBCA2 of the second layer via the contact hole 15n and thereby electrically connected to the gate electrodes 10, 10 of two pMISQps for switch element 3SW1. On the other hand, the wiring 2VSBCA3 is electrically connected to the wiring 2VSBCA2 of the second layer via the contact hole 15p and thereby connected to the gate electrodes 10, 10 of two nMISQns for switch element 3SW2. Here, the wirings 2VDBCA3, 2VSBCA3 are arranged on the third wiring layer but on the second wiring layer because of the reason that the switch elements 3SW1, 3SW2 are realized with an ordinary basic cell 1 and ~~is~~ arranged without relation to the logic to be mounted. Namely, it is not practical to form the wirings 2VDBCA and

C27 2VSBCA with the second wiring layer, because if the wirings 2VDBCA, 2VSBCA are formed with the second wiring layer, the wirings 2VDBCA, 2VSBCA forming a pair with two lines must be arranged in the X direction of the narrow basic cell 1 and thereby the wiring channels of the second wiring layer are almost destroyed. Although not illustrated in the figure, the basic cells a are coupled using the wiring of the first wiring layer extending in the X direction, wiring of the second wiring layer extending in the Y direction and wiring of the third wiring layer extending in the X direction.

Page 57:

Please substitute the following paragraph for the paragraph beginning at line 21:

C28 Moreover, also explained in this embodiment is an example where the power supply wiring 2VSS1 of the first layer is connected via the contact hole 12 to the semiconductor region 8N of unused basic cell 1 or unused nMISQn. Thereby, noise of well can be controlled only with allocation of a fine contact hole 12. Namely, even in the case of semiconductor device having the switch elements 3SW1, 3SW2, generation of noise can be controlled in the

well formed in the semiconductor substrate 4S without resulting in complicated structure and increase of chip size. Therefore, the threshold voltage of MISFET can be stabilized, latch-up can be controlled and operation reliability of semiconductor device can also be improved. The codes 11a, ~~22b~~ 11b in Fig. 22 and Fig. 24 indicate the interlayer insulation films which are formed, for example, of silicon oxide film. Moreover, the power supply wirings 2VDDA1, 2VDDA2, 2VSSA1, 2VSSA2 and wirings 2VDBCA1, 2VDBCA2, 2VDBCA3, wirings 2VSBCA1, 2VSBCA2, wirings 2VPPA1, 2VNNA1, 2LB1, 2LC1 or the like are composed of a laminated film which is formed, for example, of aluminum, aluminum alloy including silicon and copper, copper, copper alloy or a laminated film formed by laminating a conductive film of these metals and titanium nitride or titanium film.

Page 58:

Please substitute the following paragraph for the paragraph beginning at line 25:

In Fig. 25 and Fig. 26, an inverter circuit INV is arranged as the basic logic circuit and moreover the condition is schematically illustrated in which the clock circuit CL and flip-flop circuit FF are arranged as the

comparatively larger logic circuits. These logic circuits

C29 are formed of the pMISQp and nMISQn in the basic cell 1. The region other than the logic circuit region indicated with the thick frame is used as the region where the logics formed with the logic designers are arranged or as the region ~~the~~ to arrange the wiring 2. The basic cell 1 of the region to arrange the wiring 2 is the unused basic cell.

Page 59:

Please substitute the following paragraph for the paragraph beginning at line 10:

C30 The switch element 3SW indicates the simplified switch elements 3SW1, ~~2SW2~~ 3SW2. Here, the switch element 3SW is arranged in the clock circuit CL and flip-flop circuit FF. Namely, a certain logic circuit comprises a switch element 3SW, considering that a high level noise is generated momentarily and easily in the clock circuit CL and flip-flop circuit FF because ~~operate rate~~ operating speed is high, drive capability is also high and a plurality of elements or wirings are driven simultaneously. Namely, generation of noise can effectively be controlled by previously allocating the switch element 3SW within the

C30 logic circuit which easily generates noise. Moreover, in this case, in the designing stage, a logic circuit already comprising the switch element 3SW is prepared and it is then developed as the layout. Thereby, the designers can provide a layout of logic circuit without considering existence of the switch element 3SW itself. Moreover, the total or partial allocation of the switch element 3SW can be completed by providing the layout of the logic circuit comprising the switch element 3SW. Therefore, the switch element 3SW can be effectively and easily arranged and moreover it is possible to easily provide the total layout of the circuit.

Page 63:

Please substitute the following paragraph for the paragraph beginning at line 27:

C39 The power supply wirings of 2VSSD2, 2VSSD1 are arranged in the external region of the I/O cell ~~6~~ 5 to supply the power supply voltage VSS to the circuit structured with MISFET having relatively large gate width. The power supply wiring 2VSSD2 is extended like a belt in the Y direction of Fig. 31 formed in the second wiring layer. Moreover, the power supply wiring 2VSSD1 is formed

C39 in the first wiring layer and is extended like a belt in the X direction of Fig. 31. These power supply wirings 2VSSD2, 2VSSD1 are electrically connected via the contact hole 16a arranged at the crossing portion thereof.

Page 76:

Please substitute the following paragraph for the paragraph beginning at line 24:

C38 As explained above, since the nMISQnA, pMISQpA in the internal region of I/O cell 5 mainly form the input circuit and therefore the threshold voltage must relatively be lowered in order to realize higher operation rate. Therefore, since it is difficult to determine the condition during the testing period like the MISFET formed in the internal circuit region as explained above, it is necessary to provide the switch elements 3SW3 and 3SW4 and thereby to change the threshold voltage for the normal operation period and testing period. Therefore, in this embodiment, the switch elements 3SW3, 3SW4 are also provided within the region of I/O cell 5. Thereby, it is now possible to lower the threshold voltage of the pMISQpA forming the inverter circuit INV for input circuit as is designed, during the normal operation period, by turning ON the switch element

C 39

3SW3 and then applying the power supply voltage VDD to the n—well and to raise the threshold voltage of the pMISQpA forming the inverter circuit INV for input circuit, during the testing period, by turning OFF the switch element 3SW3 and then applying the voltage VPP other than the power supply voltage VDD to the n-well NWL. In the same manner, it is also possible to lower, as designed, the threshold voltage of the nMISQnA forming the inverter circuit INV for the input circuit by turning ON the switch element ~~3SW3~~ 3SW4 and then applying the power supply voltage VSS to the p-well PWL and to raise the threshold voltage of the nMISQnA forming the inverter circuit INV for the input circuit, during the testing period, by turning OFF the switch element ~~3SW3~~ 3SW4 and then applying the voltage VNN other than the power supply voltage VSS to the p-well PWL.